CLAIMS

What is claimed is:

1. A structure implementing a user circuit in a programmable logic device (PLD), the PLD including programmable logic blocks, programmable interconnect lines, and programmable interconnect points (PIPs) interconnecting the logic blocks and interconnect lines, the structure comprising:

N copies of the user circuit implemented using the logic blocks, interconnect lines, and PIPs, each copy having an output terminal, wherein N is an odd integer greater than three;

a voting circuit having an output terminal and N input terminals, wherein the voting circuit provides a value common to at least (N+1)/2 of the voting circuit input terminals at the voting circuit output terminal; and

programmable interconnections coupling the output terminals of the N copies of the user circuit to the N input terminals of the voting circuit via the interconnect lines and PIPs.

2. The structure of Claim 1, wherein the N copies of the user circuit are implemented in N distinct areas of the PLD.

3. The structure of Claim 1, wherein at least two of the N copies of the user circuit physically overlap within the PLD.

4. The structure of Claim 1, wherein the N copies of the user circuit are each implemented using the same number of logic blocks, interconnect lines, and PIPs, positioned in the same locations relative to the other logic blocks, interconnect lines, and PIPs within the same copy.

5. The structure of Claim 1, wherein N is five.

6. The structure of Claim 1, wherein the PLD is a field programmable gate array (FPGA) programmed by configuration data stored in static RAM memory cells.

7. A method of implementing a user circuit in a programmable logic device (PLD), the PLD including programmable logic blocks, programmable interconnect lines, and programmable interconnect points (PIPs) interconnecting the logic blocks and interconnect lines, the method comprising:

receiving a circuit description of the user circuit;

implementing N copies of the user circuit based on the circuit description and using the logic blocks, interconnect lines, and PIPs, each copy having an output terminal, wherein N is an odd integer greater than three;

implementing a voting circuit having an output terminal and N input terminals, wherein the voting circuit provides a value common to at least (N+1)/2 of the voting circuit input terminals at the voting circuit output terminal; and

implementing interconnections between the output terminals of the N copies of the user circuit and the N input terminals of the voting circuit via the interconnect lines and PIPs.

8. The method of Claim 7, wherein implementing N copies of the user circuit comprises implementing N copies of the user circuit in N distinct areas of the PLD.

9. The method of Claim 7, wherein implementing N copies of the user circuit comprises implementing N copies of the user circuit wherein at least two copies of the user circuit physically overlap within the PLD.

10. The method of Claim 7, wherein implementing N copies of the user circuit comprises implementing N copies of the user circuit using the same number of logic blocks, interconnect lines, and PIPs, positioned in the same locations relative to

the other logic blocks, interconnect lines, and PIPs within the same copy.

11. The method of Claim 7, wherein N is five.

12. The method of Claim 7, wherein the PLD is a field programmable gate array (FPGA) programmed by configuration data stored in static RAM memory cells.

13. The method of Claim 7, further comprising receiving from a user an indicator selecting a high-reliability implementation of the user circuit.

14. The method of Claim 7, further comprising receiving from a user a target selection indicator selecting a target PLD.

15. The method of Claim 14, wherein the target PLD is a field programmable gate array (FPGA) programmed by configuration data stored in static RAM memory cells.

16. A method of implementing a user circuit in a programmable logic device (PLD), the PLD including programmable logic blocks, programmable interconnect lines, and programmable interconnect points (PIPs) interconnecting the logic blocks and interconnect lines, the method comprising:

providing a circuit description of the user circuit; and

receiving a PLD implementation for the circuit, the PLD implementation comprising:

N copies of the user circuit implemented using the logic blocks, interconnect lines, and PIPs, each copy having an output terminal, wherein N is an odd integer greater than three;

a voting circuit having an output terminal and N input terminals, wherein the voting circuit provides a value common to at least (N+1)/2 of the voting circuit

input terminals at the voting circuit output terminal; and

programmable interconnections coupling the output terminals of the N copies of the user circuit to the N input terminals of the voting circuit via the interconnect lines and PIPs.

17. The method of Claim 16, wherein the N copies of the user circuit are implemented in N distinct areas of the PLD.

18. The method of Claim 16, wherein at least two of the N copies of the user circuit physically overlap within the PLD.

19. The method of Claim 16, wherein the N copies of the user circuit are each implemented using the same number of logic blocks, interconnect lines, and PIPs, positioned in the same locations relative to the other logic blocks, interconnect lines, and PIPs within the same copy.

20. The method of Claim 16, wherein N is five.

21. The method of Claim 16, wherein the PLD is a field programmable gate array (FPGA) programmed by configuration data stored in static RAM memory cells.

22. The method of Claim 16, further comprising providing an indicator selecting a high-reliability implementation of the user circuit.

23. The method of Claim 16, further comprising providing a target selection indicator selecting a target PLD.

24. The method of Claim 23, wherein the target PLD is a field programmable gate array (FPGA) programmed by configuration data stored in static RAM memory cells.